REMARKS

Claims 1, 7, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa et al. (English Translation of JP Patent No. 62-251917, hereinafter "Nakazawa") in view of Schnizlein (U.S. Patent No. 4,414,538, hereinafter "Schnizlein").

Applicant asserts that claims 1, 7, 16, and 17 should not be found unpatentable over Schnizlein and Nakazawa for at least the following reasons:

Lack of motivation to combine

Applicant asserts there is no motivation to combine the teachings of Schnizlein with those of Nakazawa. The Examiner stated in the Office action mailed 03/23/2007 that "it would have been obvious to a person of ordinary skill in the art to modify the teachings of Nakazawa such that the keyboard comprised a parallel-to-serial register, wherein the parallel-to-serial register is operative in response to a signal representative of a depressed key cell, as taught/suggested by Schnizlein." "The suggestion/motivation for doing so would have been because converting the parallel output data into serial output data prior to transmission to additional processing equipment would enable serial data transmission across serial links." The applicant, however, respectfully disagrees.

Firstly, Nakazawa's teachings do not require a parallel-to-serial converter because, on triggering of the scanning initiation signal (h) in Fig. 2 of Nakazawa, the discrimination means 21 scans each key sequentially. Applicant notes that second paragraph of page 6 of Nakazawa states, "it detects the condition of signal line [b, c, and d] when a signal is provided to signal lines [e, f, and g] sequentially and discriminate the depressed key. " [emphasis added] In this way, the output result of the key scanning process is already in serial form. Therefore, the key discrimination data in Nakazawa's teachings does not require a parallel-to-serial conversion because there is in fact no parallel output data to be converted into serial form. A person skilled in the art would not be motivated to include a parallel-to-serial converter since it would serve no purpose given the way Nakazawa's design functions.

Secondly, applicant asserts that there is no motivation to combine the references of

Schnizlein and Nakazawa because the teachings of Schnizlein and Nakazawa are based on different and incompatible principles of operation. The design of Schnizlein's apparatus is one that continuously scans the key matrix for key presses. Applicant points out that Schnizlein teaches in col 1, line 45-48 that their design "concerns a circuit for scanning a plurality of keyswitches arranged in a matrix having a plurality of row conductors and a plurality of column conductors." [emphasis added] On the other hand, Nakazawa's design does not scan the keyboard matrix if there is no key pressed. Applicant refers to page 4 of Nakazawa (translated), 5 lines from bottom, wherein Nakazawa's design "detects the depressed state of key using a monitor means monitoring one of contact points and checks the condition of other contact point using a discrimination means only when key depression is detected." [emphasis added] Applicant further notes that in lines 5-6 on page 7, Nakazawa (translated) states, "unless a key is depressed, the problem of delaying other processed due to the scanning operation of the discrimination means [21] never occurs." There is therefore no motivation to combine the teachings/suggestions of Schnizlein and Nakazawa due to their different principles of operation. That is, a scanning keyboard taught by Schnizlein is not compatible with a non-scanning keyboard that prevents the problems resulting from the scanning operation as taught by Nakazawa.

Combination does not teach all features of present invention

Concerning independent claim 1, even if the parallel-to-serial converter 64 of Schnizlein's teachings were included into the design of Nakazawa, applicant asserts that the resulting combination would not include at least the following feature as claimed in claim 1 of the present invention:

"a parallel-to-serial register electrically connected to the output end of the key module" [claim 1 - emphasis added]

The reason is that Schnizlein's teachings connect the parallel-to-serial converter 64 to a ROM decoder 66 and debounce and validation logic 62, neither of which is equivalent to the output of the key module as is claimed in claim 1 of the present invention. Additionally, applicant points out that both the ROM decoder 66 and the

debounce and validation logic 62 are required by the design of Schnizlein in order to determine a representation of the scanned keyswitch that is depressed and to achieve both key debounce and an N-Key rollover feature. Note that col 4, lines 10-12 state, "the ROM decoder 66 provides a parallel output signal on a multi-line cable 67 representing the scanned keyswitch to the parallel to serial converter 64"; col 4, lines 2-3 state, "The debounce and validation logic 62 serves to distinguish between extraneous signals and valid key closures"; and col 4, lines 5-6 of Schnizlein state, "The debounce and validation logic unit 62 may include an N-Key rollover feature." Therefore, a person skilled in the art would not electrically connect the parallel-to-serial register to the output end of the key switches 16a-y of Schnizlein's design because in doing so they would no longer be following the teachings of Schnizlein and would no longer be able to achieve the many benefits as taught by Schnizlein.

Furthermore, as quoted above, Nakazawa teaches in the second paragraph of page 6 sequentially providing signals to signal lines e, f, and g while detecting the condition of signal lines b, c, and d in order to discriminate the depressed key. Therefore, the output ends of the key module 10 (i.e., signal lines b, c, and d) in Fig. 2 of Nakazawa need to be monitored in conjunction with input signal lines e, f, and g, and it would not make sense to couple a parallel-to-signal converter to the output of the key module 10 (i.e., signal lines b, c, and d) as further logic needs to be performed on these signal lines for discriminating the depressed key. In view of Schnizlein, the inclusion of a parallel-to-serial converter into Nakazawa's design would require the discrimination means 21 to first perform logic on the output signals from signal lines b, c, and d. And therefore, if for some reason a parallel-to-serial converter was to be added, it would need to be coupled to the discrimination means 21 and not to the output end of the key module 10 (i.e., signal lines b, c, and d) as is claimed by present invention.

In summary, neither Schnizlein nor Nakazawa teach/suggest a parallel-to-serial converter electrically connected to the output end of the key module, as is claimed in claim 1 of the present invention. Therefore, applicant asserts that a combination of Schnizlein and Nakazawa would also not teach or suggest this feature. For at least this reason applicant asserts that claim 1 should not be found unpatentable in view of

Schnizlein and Nakazawa. Reconsideration of claim 1 is respectively requested. Similar arguments also apply to independent claim 16 of the present invention.

Concerning claim 7 of the present invention, applicant asserts that neither Nakazawa nor Schnizlein teach the following feature as claimed in claim 7 of present invention:

"a detect circuit electrically connected to the output end of the key cell for detecting a transient voltage at the moment when the key cell is pressed or released and then generating a control signal" [emphasis added]

The Examiner stated in the same Office action that Nakazawa teaches "detecting a transient voltage at the moment when the key cell is pressed or released, resulting in a potential decrease from +5 V to 0 V, and then generating a control signal" [emphases added]on pages 5-6, 8. Applicant, however, respectfully disagrees and notes that Nakazawa teaches only monitoring the signal voltage (page 6, line 9-12) and not a transient voltage: "if the signal line (a) is +5 V, it indicates that no key is pressed; whereas if the signal line (a) is 0 V, it indicates that some key has been depressed." The teaching of Nakazawa detects the static voltage on the signal line and asserts the scanning initiation signal (h) when the signal line voltage (a) is 0 V, but does not reset the scanning initiation signal (h) if the signal line voltage (a) remains unchanged at 0 V; that is, the scanning initiation signal (h) of Nakazawa remains asserted even when there is no transient voltage on signal line (a). On the other hand, the principle of operation in the present invention monitors a signal (the transient voltage) deriving from the change in voltage at the output end of a key cell. The present invention invokes the control signal only when a key in the keyboard "changes state"; that is, only when a key is pressed, or when a key that was previously pressed is released.

With respect to the "at the moment" limitation of claim 7, it should be noted that the debounce logic as shown by Schnizlein requires at least two successive scans of the complete key matrix in order to determine whether a key has actually been depressed and that the signal received is not simply noise. Schnizlein teaches in col 4, line 38-42 that: "After successive scans of the closed keyswitch 16C, the debounce and validation logic

62 sends a signal to the converter 64 which in turn provides an encoded serial signal to an external device (not shown)." [emphasis added] This procedure means output from the coding circuit is not "at the moment" of the key press, as is the case in the present invention. The same remark can be said of Nakazawa's design when a key has already been pressed, where in lines 5-6 from the bottom of page 6, Nakazawa states the "scanning operation may be the same process as the conventional device". [emphasis added] In the present invention, however, the control signal triggers an immediate parallel input of the output ends of all the key cells within the key module 52 without the need for additional scan progressions before the parallel-to-serial converter can output resultant data. Furthermore, the debounce and validation logic process from Schnizlein's teachings can cause the occurrence of a key pressed and released in rapid succession to be discarded as "noise" (if pressed, then released before the second successive scan detects its depressed state).

Moreover, neither Schnizlein nor Nakazawa teach detecting and utilizing a key release to assert the control signal. In both the designs of Schnizlein and of Nakazawa, a key that is released does not initiate a read or discrimination process from the key cell output ends. Additionally, neither Schnizlein nor Nakazawa teach designs that initiate a key discrimination process triggered by a control signal resulting from both key presses as well as key releases. The present invention is able to detect both key presses and key releases in the same circuit and operation.

For at least these reasons, applicant asserts claim 7 should also not be found unpatentable over Nakazawa and Schnizlein. Similar arguments also apply to independent claim 17.

Concerning claims 16 and 17, in addition to all the arguments provided above for claim 1 and claim 7, respectively, applicant would also like to point out that while in Schnizlein's design the parallel-to-serial register continues to receive input data from the output end of the key cell when a key cell is released, Nakazawa's design does not, and modifying Nakazawa in view of Schnizlein will negate the non-scanning advantages of Nakazawa's design over the prior art admitted by Nakazawa. In this way, a combination

of Schnizlein and Nakazawa would not operate to determine and identify when a key is released, and therefore would also not include a parallel-to-serial register for inputting input data from the output end when the key cell is pressed or released, as is claimed in claim 16 and 17 of the present invention. For at least these reasons, applicant asserts claims 16 and 17 should also not be found unpatentable over Nakazawa and Schnizlein.

Accordingly, the applicant believes that the Examiner has no grounds to combine the Schnizlein and Nakazawa references to render claims 1, 7, 16 and 17 of this application unpatentable. Firstly, there is no motivation to combine the references as Nakazawa does not include parallel output data, and unlike Schnizlein, functions using a non-scanning principle of operation. Even if combined, as described above, applicant asserts that it is impossible for a person skilled in the art to achieve the same functions and components as claimed in the present invention claims 1, 7, 16 and 17 without further inventive process. The reason is there are several features claimed by the present invention that are not present in either of the cited references of Schnizlein and Nakazawa. For at least these reasons, applicant asserts claims 1, 7, 16 and 17 of the present invention should be found patentable over Nakazawa and Schnizlein. Reconsideration of claims 1, 7, 16 and 17 is respectfully requested. Claims 2-6 and 8-15 are dependent upon claims 1 and 7 and should therefore be found allowable for at least the same reasons. Additionally comments regarding the patentability of particular dependent claims is provided in the below sections.

Claims 2, 3, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa et al. (English Translation of JP Patent No. 62-251917) and Schnizlein (U.S. Patent No. 4,414,538) as applied to claims 1, 7, 16, and 17 above, and further in view of Hackmeister (U.S. Patent No. 4,027,306, hereinafter "Hackmeister").

As mentioned above, claims 2,3 and 8-10 are dependent upon claims 1 and 7, respectively, which are believed to be allowable for the above stated reasons. Therefore, claims 2,3 and 8-10 should also be found allowable for the same reasons as their base claims.

Additionally, applicant asserts there is no motivation to combine the teachings of Hackmeister with those of Nakazawa and Schnizlein because Hackmeister does not use key switches. The reason Hackmeister includes a capacitor 26 is to transfer a small voltage induced by a person's finger touching ohmic contact 13'. See col 4, lines 9-13 stating, "When a person touches the ohmic contact 13', the small voltage induced in his person by electromagnetic fields present in the environment is conducted via the capacitor 26 to the high impedance input terminal 27 of the amplifier 28." In a design including switches for keys as in Nakazawa and Schnizlein, there would be no need to include a capacitor 26 as the voltage caused by pressing the key switch is much larger. For example, connecting the output end of the switch to either ground or power voltage levels. Additionally, Hackmeister teaches the amplifier is required also because of the weak induced voltage from the person's finger. See col 4, lines 14-18 stating, "The gain of the amplifier 28 is sufficient to amplify the weak induced voltage (typically between about 50 millivolts and about 1 volt) to a level applicable for use in standard integrated circuit of transistor logic." Applicant notes that if switches were utilized for the keyboard, as in the designs of Nakazawa and Schnizlein, there would be no need to amplify the signals resulting from pressing the key switches as the resulting signals would already be at levels applicable for use in standard integrated circuit. The fact that Nakazawa and Schnizlein operate without capacitors 26 and amplifier 28, and do not suffer any ill effects of doing so serves as further proof that a person of ordinary skill would not be motivated to add these unnecessary components to achieve no noticeable benefit (ie., the designs of Nakazawa and Schnizlein operate just as well without the capacitor 26 and amplifier 28 as they would if they were included).

For at least these reasons, applicant asserts there is no motivation to combine the teachings of Hackmeister with Nakazawa, and there is also no suggestion/motivation to integrate the teachings of the Hackmeister reference with a combination of Nakazawa and Schnizlein references, if such a combination may itself be established, to achieve the present invention as claimed. For at least these reasons, claims 2, 3, 8 and 10 of the present invention should not be found unpatentable over Nakazawa and Schnizlein, and further in view of Hackmeister. Reconsideration of claims 2, 3, 8, and 10 is respectfully

requested.

Claims 4-6 and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa et al. (English Translation of JP Patent No. 62-251917), Schnizlein (U.S. Patent No. 4,414,538) and Hackmeister (U.S. Patent No. 4,027,306) as applied to claims 1-3, 7-10, 16, and 17 above, and further in view of Johnson (U.S. Patent No. 6,265,993 B1, hereinafter "Johnson").

As mentioned above, claims 4-6 and 11-15 are dependent upon claims 1 and 7, respectively, which are believed to be allowable for the above stated reasons. Therefore, claims 4-6 and 11-15 should also be found allowable for the same reasons as their base claims.

New claims 18-26

Applicant has added new claims 18, 19, 20 and 21 being dependent on claims 1, 7, 16 and 17, respectively. Further limitations of the parallel-to-serial register are added in the new claims. Specifically, the connection of the parallel-to-serial register to a plurality of key cells is detailed, and the parallel-to-serial register is for reading parallel input being the voltages at the output end of all the key cells and converting the parallel input into serial representation for output to the processor. No new matter is entered. In particular, the applicant points out that the connection of the parallel-to-serial register to a plurality of key cells is fully disclosed in figure 2 as originally filed and the operation of the parallel-to-serial register is fully disclosed in paragraph [0017] of the present invention as originally filed. Concerning the patentability, applicant asserts that the claimed structure and operation is different than the cited references and should therefore be found allowable in view of said references. Specifically, the parallel-to-serial unit of Schnizlein does not perform the same function as in the present invention. Schnizlein teaches it outputs serial form of the code corresponding to the key if it is depressed. In present invention, the parallel-to-serial register outputs the state of all keys at the moment that one key is pressed or released.

Applicant has also added new claims 22, 23, 24, 25 being dependent on claims 1,

7, 16 and 17, respectively. Further limitations of detect circuit are added. Specifically, the detect circuit is also for detecting a transient voltage being greater than a reference voltage, both at the moment the key cell is pressed and at the moment the key cell is released; and that the transient voltage is a voltage spike that occurs at the moment the key cell is pressed and released. No new matter is entered. In particular, such operation is fully disclosed in Figure 3 of the present invention as originally filed. Concerning the patentability, applicant asserts that the detect circuit and transient voltage as claimed are different than that of the cited references and should therefore be found allowable in view of said references.

Finally, applicant has added new independent apparatus claim 26. No new matter is entered. In particular, the keyboard circuit structure claimed in new claim 26 is fully disclosed and corresponds directly to that shown in Figure 2 of the present invention as originally filed. Concerning the patentability, applicant asserts that the structure of Fig.2 of the present invention is different than that of the cited references and should therefore be found allowable in view of said references.

Conclusion:

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,

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